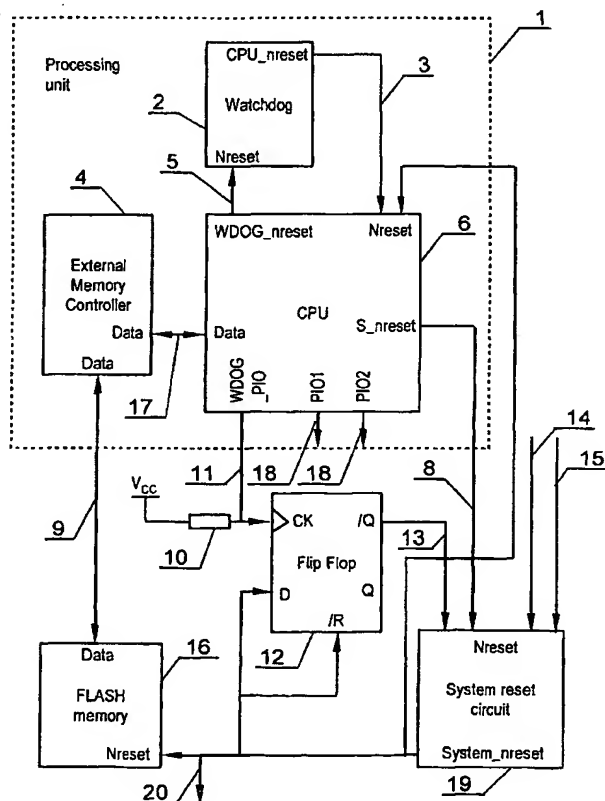




(10) International Publication Number
WO 2004/003714 A2

- [Continued on next page]*

(57) Abstract: In a circuit for detection of internal microprocessor watchdog device execution comprising a microprocessor (6) with the internal watchdog device and with an input/output line (11) transmitting information about microprocessor reset, and a device for resetting the microprocessor system, to the input/output line (11) transmitting information about microprocessor (6) reset, a clock input CK is connected, which triggers the flip-flop (12), whose data input D and an inverted reset input /R are connected to the output of the device (19) for resetting the microprocessor system, and the inverted flip-flop (12) output /Q is connected to the input of the device (19^A) for resetting the microprocessor system.





ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

— of inventorship (Rule 4.17(iv)) for US only

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for all designations
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations

Published:

- without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.